Appl. No. 10/612,479
Rule 312 Amdt. dated Jun. 13, 2006
After Not. of Allow. and Fee(s) Due of Apr. 10, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-22 (cancelled).

23. **(currently amended)** A memory circuit in single-port memory structure having a predetermined memory access speed and a memory access period, comprising:

memory cells disposed to store data; and

a circuit arranged to provide predecoding at a speed substantially faster than the predetermined memory access speed, and allowing access to a selected memory cell at least twice during the memory access period, thereby providing dual-port functionality ~~thereby~~.

24. (previously presented) The memory circuit of Claim 23, wherein the memory cells are arranged in groups and wherein each of a designated group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

25. (previously presented) In a single-port memory structure having local and global data sensing, local and global location selecting, and memory modules having groups of memory cells and a memory location, and wherein storage of a second datum at a designated memory location is to follow sensing of a first datum at the designated memory location, a method for substantially simultaneously retrieving a first datum from the designated memory location in the memory module and storing the second datum in the redundant memory location, the method comprising:

(a) locally selecting the designated memory location from which the first datum is to

be retrieved;

(b) locally sensing the first datum in the designated memory location;

(c) assigning a redundant memory location to represent the designated memory location;

(d) globally selecting the redundant memory location for storing the second datum;

(e) substantially concurrently with the globally selecting, globally sensing the first datum in the designated memory location;

(f) outputting the first datum subsequent to the globally sensing;

(g) inputting the second datum substantially immediately subsequent to the outputting the first datum;

(h) locally selecting the redundant memory location for storing the second datum; and

(i) storing the second datum in the redundant memory location.

26. (previously presented) The method of Claim 25, further comprising precharging bitlines coupled with the memory location, prior to locally sensing the first datum.

27. (previously presented) The method of Claim 26, wherein steps (a) through (i) are completed within one access cycle of the memory structure.

28. (previously presented) The method of Claim 27, wherein at least the steps of locally sensing, storing the second datum and precharging are completed within one access cycle of the memory structure.

29. (previously presented) A method for substantially simultaneously retrieving a first datum from a first memory and storing a second datum in a second memory location, wherein

both locations are disposed within a single-port memory structure having local and global data sensing, and local and global location selecting, the method comprising:

a. locally selecting the first memory location from which the first datum is to be retrieved;

b. locally sensing the first datum in the first memory location;

c. globally selecting the second memory location;

d. substantially concurrently with the globally selecting, globally sensing the first datum at the first memory location;

e. outputting the first datum subsequent to the globally sensing;

f. inputting the second datum substantially immediately subsequent to the outputting the first datum;

g. locally selecting the second memory location; and

h. storing the second datum in the second memory location.

30. (previously presented) The method of Claim 29, further comprising precharging bitlines coupled with the first and the second memory locations, prior to locally sensing the first datum.

31. (previously presented) The method of Claim 30, wherein steps (a) through (h) are completed within one access cycle of the memory structure.

32. (previously presented) The method of Claim 31, wherein at least the steps of locally sensing, storing the second datum and precharging are completed within one access cycle of the memory structure.

33. (previously presented) The method of Claim 29, wherein the first memory location is the same as the second memory location.

34. (previously presented) A method for providing sequential storage of a first datum in a first memory structure location and a second datum in a second memory structure location within one access cycle of the memory structure, the structure having local and global location selecting, the method comprising:

(a) selecting the first memory structure location to which the first datum is to be stored;

(b) precharging bitlines coupled with the memory cells at the first memory structure location;

(c) storing the first datum in the first memory structure location;

(d) selecting the second memory structure location to which the second datum is to be stored;

(e) substantially concurrently with the selecting the second memory structure location, precharging bitlines coupled with the second memory structure location; and

(f) storing the second datum in the second memory structure location.

35. (previously presented) The method of Claim 34, wherein (a) through (f) are completed within one access cycle of the memory structure.

36. (previously presented) The method of Claim 35, wherein at least the steps of storing the first datum, precharging bitlines and storing the second datum are completed within one access cycle of the memory structure.

37. (previously presented) The method of Claim 34, wherein the first memory structure location is the same as the second memory structure location.

38. **(currently amended)** A single-port memory structure having a predetermined memory access speed and a memory access period, comprising:

(a) memory cells disposed to store data;

(b) global row decoders of selected ones of the memory cells; and

(c) a predecoding circuit coupled with selected global row decoders, wherein the predecoding circuit is disposed to provide predecoding at a speed substantially faster than the predetermined memory structure access speed, and allowing access to a selected memory cell at least twice during the memory access period, thereby providing dual-port functionality ~~thereby~~.

39. **(currently amended)** The single-port memory structure of Claim 38, wherein the predecoding circuit is disposed to provide predecoding at a speed more than twice the predetermined memory structure access speed, and allowing access to a selected memory cell three or more times during the memory access period, thereby providing multi-port functionality ~~thereby~~.